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Review

An Electromagnetic Perspective of Artificial Intelligence Neuromorphic Chips

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Abstract — The emergence of artificial intelligence has represented great potential in solving a wide range of complex problems. However, traditional general-purpose chips based on von Neumann architectures face the "memory wall" problem when applied in artificial intelligence applications. Based on the efficiency of the human brain, many intelligent neuromorphic chips have been proposed to emulate its working mechanism and neuron-synapse structure. With the emergence of spiking-based neuromorphic chips, the computation and energy efficiency of such devices could be enhanced by integrating a variety of features inspired by the biological brain. Aligning with the rapid development of neuromorphic chips, it is of great importance to quickly initiate the investigation of the electromagnetic interference and signal integrity issues related to neuromorphic chips for both CMOS-based and memristor-based artificial intelligence integrated circuits. Here, this paper provides a review of neuromorphic circuit design and algorithms in terms of electromagnetic issues and opportunities with a focus on signal integrity issues, modeling, and optimization. Moreover, the heterogeneous structures of neuromorphic circuits and other circuits, such as memory arrays and sensors using different integration technologies, are also reviewed, and locations where signal integrity might be compromised are discussed. Finally, we provide future trends in electromagnetic interference and signal integrity and outline prospects for upcoming neuromorphic devices.

Keywords — Signal integrity, Electromagnetic interference, Electromagnetic design, Neuromorphic chips, Heterogeneous integration.
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I. Introduction

Artificial intelligence (AI), which was formally proposed in the 1956 Dartmouth Conference [1], is a technology that imitates and expands human intelligence. It is currently in a third wave of development. The emergence of AI shows great promise in solving a wide range of complex problems in science, engineering, finance, security, education, transportation, and logistics, to name a few. In recent years, global digital innovation has revived a new upsurge in AI research and applications. Based on the efficiency of the human brain, which consists of more than 10^{11} neurons and 10^{15} synapses and consumes only 20 watts, much research has demonstrated that neuro-inspired computing chips are able to emulate the working mechanism and the neuron-synapse structure of the brain [2], which are named neuromorphic chips. Therefore, neuromorphic chips are able to provide better performance in terms of energy efficiency and computing capabilities when performing AI tasks.

Traditionally, the general-purpose chips mostly use the architecture of computing units and storage units separated from each other, namely, the von Neumann architecture. Therein, computing units need to frequently access a large amount of data in the storage unit to perform AI operations based on the big data. The resulting operational speed is often limited by the memory read and write speed, which results in a "memory wall" [3]. Hence, the computational and storage demands of these complex algorithms exceed the capabilities of central processing unit (CPU)-based platforms. On the other hand, the graphical processing units (GPUs), field programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs) have demonstrated their superior capabilities in many areas. However, these devices also face a great challenge due to their use of the von Neumann architecture, especially in typical sensor-rich designs (such as autonomous vehicles, robotics, and wearable electronics) and low-delay requirement designs (such as real-time applications). Therefore, development of neuromorphic chips has become a great interest to an increasing number of leading scientific research institutions

and companies around the world.

The existing neuromorphic chips are designed to accelerate AI algorithms; however, partially chips realize biological characteristics of the human brain neural network [4]. To further improve the computational efficiency of neuromorphic chips and reduce the power consumption, it is necessary to more deeply imitate the behavior of human brain neural networks in the future, including human brain neural signals and neural network architecture. In particular, the imitation of spiking neural networks (SNNs), which are considered the third generation of neural networks [5], further advances emulation of the human brain by using spikes to exchange information between neurons and adapting neurons to work on event-driven networks, i.e., when the potential of a neuron reaches a threshold, it emits a spike, while other neurons remain idle. This concept of spatiotemporal event representation contributes to energy efficiency in SNN-based applications, based on which there have been preliminary explorations in hardware implementation, that is, spiking neuromorphic chips [6]. Spiking neuromorphic chips have the characteristics of low power consumption, low latency, high-speed processing, and space-time integration. This represents a promising long-term development direction for neuromorphic chips.

With the complexity of neuromorphic chips, the electromagnetic problem such as electromagnetic interference (EMI) and signal integrity (SI) issues will pose a great challenge to early stage chip design. EMI- and SI-related research on neuromorphic chips promotes development toward high speed, integration, and intelligence, which has important scientific value and industrial application prospects. Thus, this paper provides a comprehensive review on EMI and SI concerns specific to neuromorphic chips. It is preceded by an introductory overview of neuromorphic chips, encompassing their design principles, algorithmic frameworks, and practical applications. Acknowledging the distinctive characteristics of memristor-based chips, we introduce the EMI and SI challenges associated with these diverse memristor-based architectures in a dedicated subsection. Another main topic we discuss in this review is the EMI and SI aspects relevant to various heterogeneous integration (HI) structures for neuromorphic chips, encompassing printed circuit boards (PCBs), systems-on-chips (SoCs), 3D configurations, and optical connections.

The remainder of this paper is organized as follows: Section II reviews the circuit design and applications of neuromorphic chips, while Section III illustrates the EMI and SI issues in neuromorphic chips based on complementary metal oxide semiconductor (CMOS) and memristor devices. Section IV explains the design of different HI structures of neuromorphic and other chips and analyzes the EMI and SI issues. In Section V, we discuss various techniques for EMI and SI analysis and optimization and future prospects. Finally, Section VI offers conclusions.

II. Review of Neuromorphic Circuit Design and Application

To ensure that a functional chip is able to function properly in a complex electromagnetic environment, its immunity to SI and EMI issues are essential indicators [7]–[9]. Due to the unique hardware architecture and biological design concept, the neuromorphic chip is considered to have high parallelism, low power consumption, and robustness, making it also an emerging technology of interest in the future of computing [10]. While von Neumann computers encode information as numerical values represented by binary values, neuromorphic chips use spike sequences as input and output. Much work has been done to optimize the hardware architecture of neuromorphic chips with different designs to better adapt their characteristics [11]–[14]. Here, we briefly review the design aspects of large-scale neuromorphic chips, resistive random-access memory (RRAM) devices, and their computation algorithms and applications. Moreover, we highlight the potential advantages of neuromorphic chips in different applications.

1. Circuit design

Neuromorphic chips can be achieved through digital implementation or mixed analog-digital implementation. The effort of the neuromorphic hardware design was initiated by many research institutions, followed by partnerships with the industry, as illustrated in Figure 1. The University of Manchester developed a purely digital neuromorphic chip called SpiNNaker [15] with two versions (SpiNNaker and SpiNNaker2). Similarly, Zhejiang University and Zhejiang Lab developed the Darwin Neuromorphic Processing Unit (NPU) [12], a digital chip with off-chip memory to store synapse information. IBM and Intel also developed two digital neuromorphic chips known as TrueNorth [16] and Loihi [17], respectively. Stanford University's Neurogrid [18] and Braindrop [19] are examples of the mixed-analog-digital systems, and the neurons are designed using analog circuits. Another mixed-analog-digital design is BrainScaleS [20], from the University of Heidelberg and Technische Universitat Dresden. In 2015, Tsinghua University introduced a cross-paradigm neuromorphic digital chip called Tianjic, which integrates artificial neural networks (ANNs) and SNNs into hybrid neural networks (HNNs) [4].

RRAM devices have experienced rapid development in the past two decades. Figure 2 shows that RRAM was first proposed in 2008 as the missing fundamental element in Berkeley [24]. Since then, many researchers attempted to fabricate real RRAM devices as well as developing underlying physical principles. From 2017 to 2021, large companies such as IBM and Intel and foundries such as TSMC started to tape out some RRAM samples compatible with CMOS process nodes. At the same time, many researchers started to develop RRAM Macro [25] and system integration. During the past two years, 3D integration of 3D-RRAM [26], programmable RRAM chips and SoC [27], [28] with RRAM has been achieved with impressive energy and area efficiency. Some start-ups also announced the release of their commercial products based on RRAM at the end of 2023. The trend of the development of RRAM chips in the

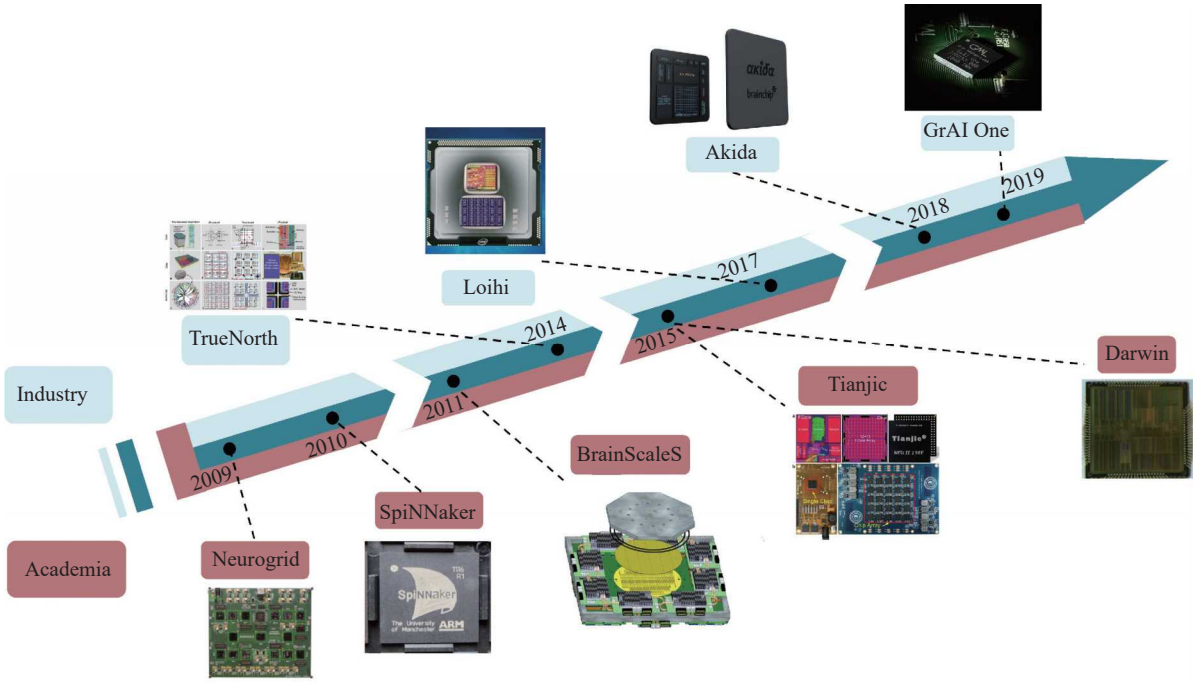

Figure 1 During the last four decades of the neuromorphic field, several neuromorphic chips have been developed. Popular large-scale neuromorphic chips and their first reported years: as early as 2009, Stanford University released the Neurogrid [18] neuromorphic chip. In 2010 and 2011, the first versions of SpiNNaker [15] and BrainScaleS [21] were released for the first time by University of Manchester and Heidelberg University, respectively. In 2014, IBM released its neuromorphic chip, TrueNorth, which has 4096 neuro-synaptic cores, with 1 million neurons and 256 million synapses [11]. A year later, in 2015, the first generation of the Tianjic chip, which was the first hybrid chip that can use both ANN and SNN, was developed by Tsinghua University [4]. In the same year, the first generation of Darwin NPU was developed by Zhejiang University and Zhejiang Lab [12]. In 2017, Intel Labs developed the first generation of Loihi chips with 130 thousand neurons and 130 million synapses [17]. BrainChip's Akida was the first commercial neuromorphic chip in 2018 [22]. In 2019, GrAI Matter Labs presented GrAI One chip [23] that is capable of accelerating both ANN and SNN.

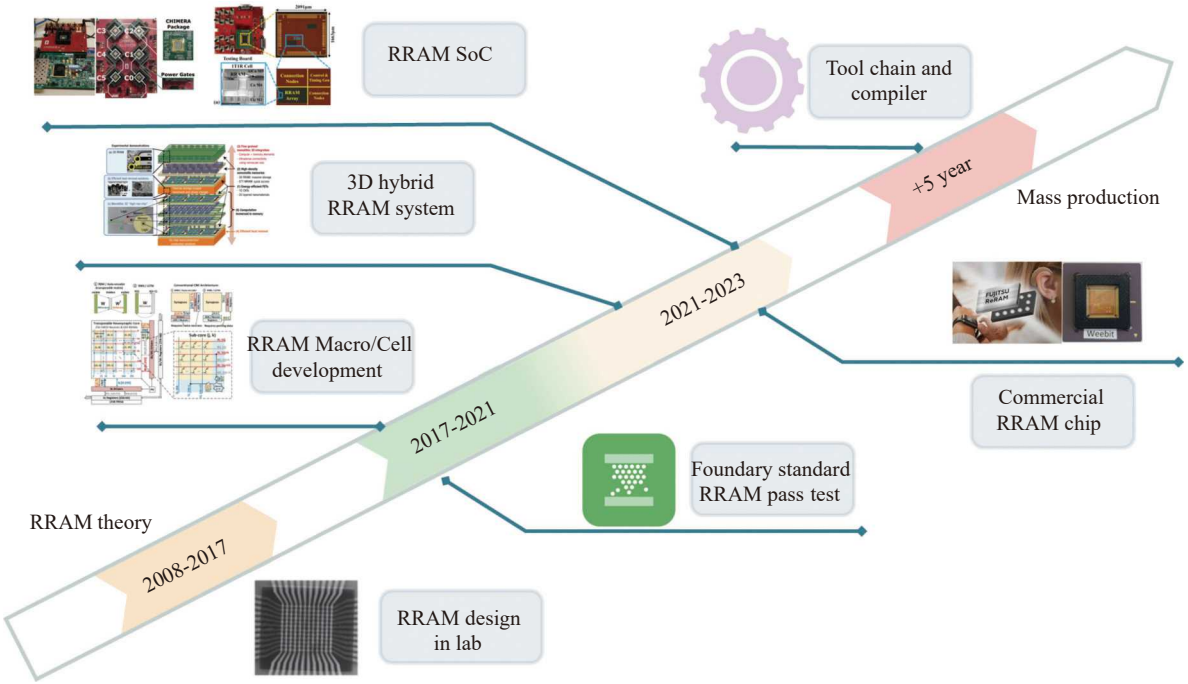

Figure 2 RRAM device development in a nutshell: in 2008, the first RRAM was proposed. From 2017 to 2021, many companies started RRAM devices compatible with CMOS technology [25]. Recently, 3D-RRAM was realized, which dramatically improved the energy and energy efficiency [26]. In the next few years, the focus is expected to be on the related tool chain and compilers, efficient SoC design and 3D integration compatibility.

next five years may focus on related tool chains and compilers, efficient SoC design and 3D integration compatibility. Figure 3 shows the typical neuromorphic chips layout and architecture.

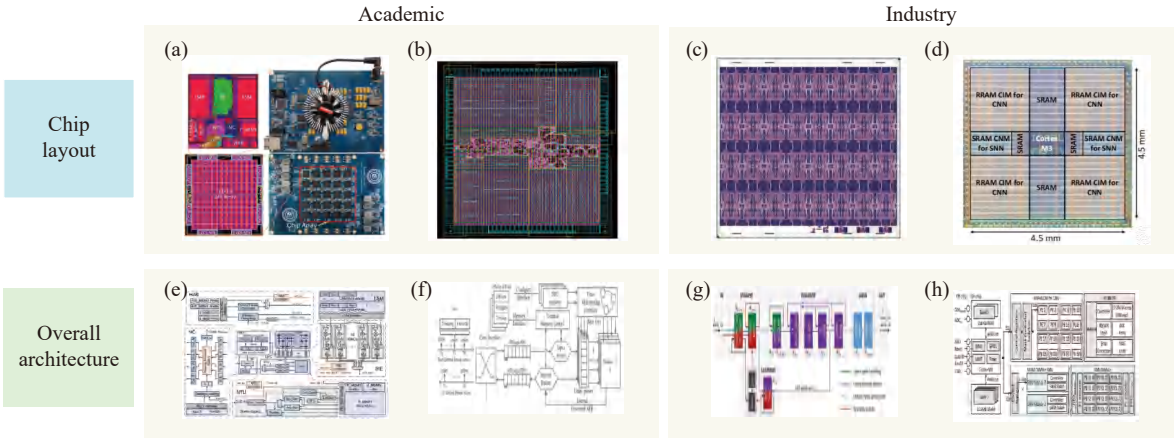

Figure 3 Typical neuromorphic chips by academic and industrial communities. (a) and (e) Tianjic neuromorphic chip for SNN/DNN workload [4]; (b) and (f) Darwin neuromorphic chip [12]; (c) and (g) Intel's Loihi for SNN [17]; (d) and (h) ReRAM/SRAM hybrid CIM for SNN/DNN by TSMC [29].

As mentioned, neuromorphic chips are advantageous over CMOS-based chips in terms of energy consumption, low latency, high-speed processing, and space-time integration. Moreover, analog devices such as memristors help to scale down the device size to sub-2 nm [30] and integrate into high-density 3D arrays [31]. Although the development of these technologies is still considered in its early stages, a key challenge is related to the development of large-scale chips based on nonvolatile memory (NVM) [2]. This challenge leads to urgent and extensive research on NVM-based chips from the device to chip level. At the device level, the weight tuning precision depends on how many analog states a memristor has. Other factors, such as the on/off ratio of the analog switching regime, the linearity of the conductance tuning, and the symmetry in the trajectory of the weight increase and decrease, must be considered. Reliability issues are also critical for neuromorphic chips. As weight tuning sometimes requires a large number of operations in each cell, its endurance is a determinant of its performance.

At the circuit level, crossbar array structures are used for vector-matrix multiplications (VMMs), where the matrix is mapped onto a memristor-based crossbar, and the weights are stored as memristor conductance. In Subsection III-2, memristor-based neuromorphic crossbar arrays are further explored and reviewed, especially for EMI and SI issues due to parasitic elements.

2. Algorithm

1) Neural coding

Figure 4 shows the key attributes of biological and silicon-based computing frameworks [32]. As mentioned earlier, using spike sequences as input and output is an essential feature of neuromorphic computation. Therefore, implementing a numerical-to-pulse sequence encoder and decoder is a fundamental module for deploying neuromorphic algorithms for a given task. There are two mainstream techniques to encode spikes: rate encoding, which carries information through the frequency of spike issuance within a certain length of the time window, and temporal encoding, which encodes temporal information on spiking [33]. A most widely used frequency coding methods is Poisson coding, which encodes the normalized numerical information as a spike sequence with the number of spike releases conforming to the Poisson process. Due to the concept of randomness inherent in such encoders, when noise affects a single spike, the whole computing system has a natural robustness advantage. A typical approach to temporal coding would be to characterize the information using the exact moment when the spikes are issued in a time window. In addition, various coding methods, such as differential and phase coding, have been further proposed to improve the encoder's performance by incorporating communication modulation theory.

The spike decoding method generally corresponds to the encoding method, for example, by counting the spike delivery rate over time to obtain the rate of encoding information or by locating the exact time of spike delivery to restore the original information from the temporal encoding. However, it is also worth mentioning that in practical application scenarios, the neuromorphic chip may receive spike input directly, for example, when a dynamic vision sensor is used as signal input instead of a conventional optical camera [34], [35]. In this case, the spike signal contains more spatiotemporal information, and the decoder needs to be further discussed and selected in combination with the neuromorphic computing algorithm used.

The low power consumption characteristics of the neuromorphic chip are also related to its use of spike sequences as data streams. Similar to how the human brain functions, the event-driven nature allows the circuitry of the neuromorphic chip to be idle most of the time without receiving new spikes from the previous synapses. In addition, due to the dual characteristics of the spikes, the corresponding neural computation algorithm reduces many multiplication operations to fewer operations, which can further reduce the computational overhead. The low-power effects also make the neuromorphic chip expected to better mitigate

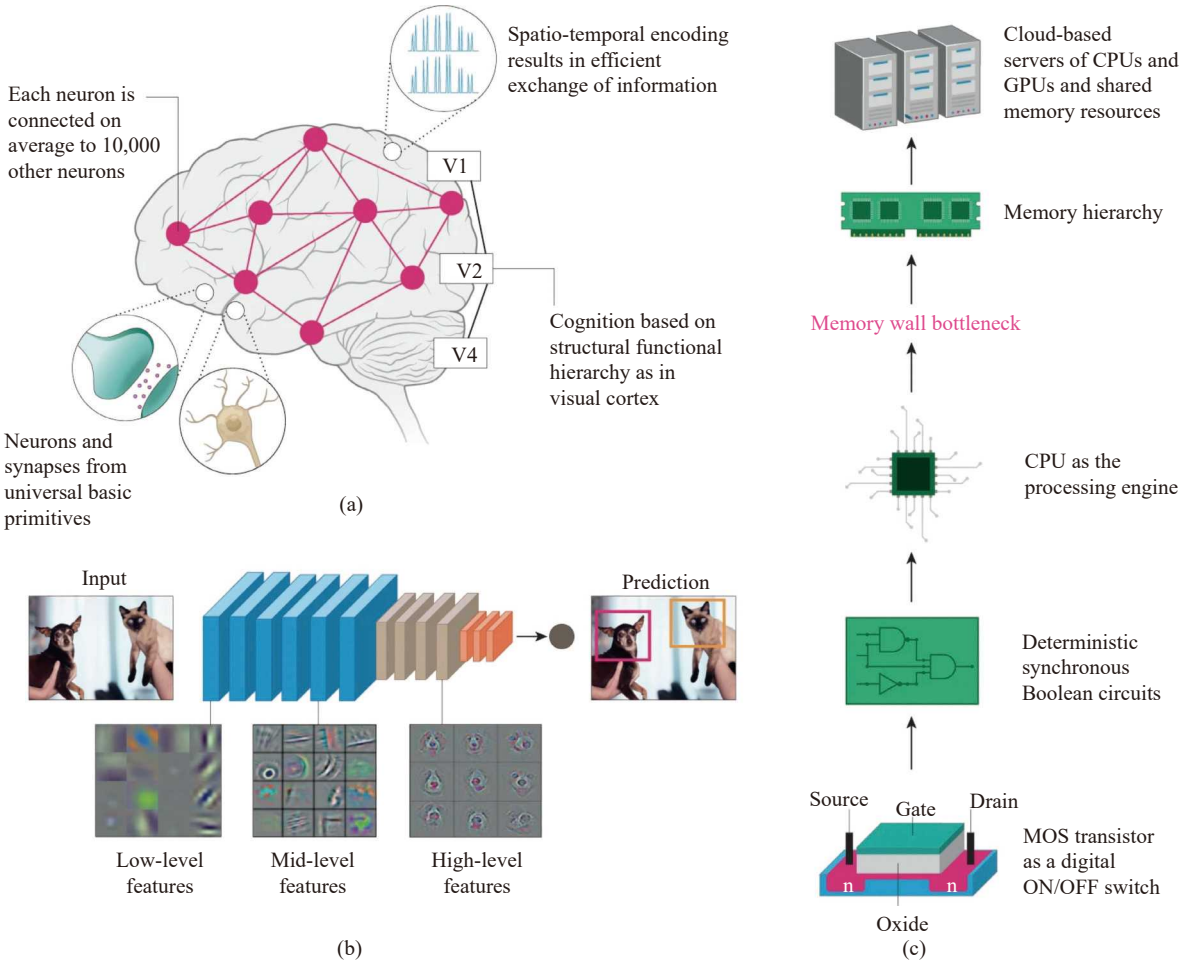

Figure 4 Key attributes of biological and silicon-based computing frameworks [32]. (a) A schematic of the organizational principles of the brain; (b) A deep convolutional neural network performing objection detection on an image; (c) A state-of-the-art silicon computing ecosystem.

EMI problems.

2) Neuronal dynamics

In recent years, the development of machine learning, especially ANNs, and the development of many applications are important reasons for the surge in demand for chip computing power. For applications of large natural language processing models, the parameter quantity of the neural network model has reached 100 billion [36]. Another more severe challenge is how to train such a large-scale neural network. Even if the equipment requirements and energy overhead required for training are addressed, there is still a need to ensure good parallelism among thousands of GPUs to enable the load to be operated efficiently and to be scalable at both the memory and computation levels.

Research in the field of neuromorphic computing is expected to be inspired by the human brain to develop next-generation computers. The mainstream algorithmic framework in neuromorphic computing is SNNs, which originated from the theoretical foundation of neuroscience and is also considered the third generation of neural networks [37]. Figure 5 shows some similarities and differences between ANN and SNN when simulating biological neurons. Compared with ANN, SNN uses a spike encoder and decoder at the input and output ends, respectively. Such an internal computing unit is modeled on the neuron structure and reproduces the unique neuronal dynamics. When handling the complex relationship between input and output, ANN neurons exhibit nonlinear fitting with the help of activation functions such as rectified linear units (ReLUs). Simultaneously, SNNs are based on biological neurology and introduce dynamic characteristics such as membrane potential accumulation, leakage, and fire. The neuronal dynamic of the SNN is also an adaptive result because the information density of the spike data stream is less than that of the ANN. Therefore, it is usually necessary to rearrange and analyze the spike sequences within a certain time window to achieve similar functions [38]. In addition, neuron dynamics make the activity of each neuron depend on its membrane potential and spike fire rules, so the whole network is well parallelized in its deployment. At the same time, each neuron has its unit to store the state of the membrane potential, thus presenting storage and computational integration throughout the computational model to break the computational performance bottleneck.

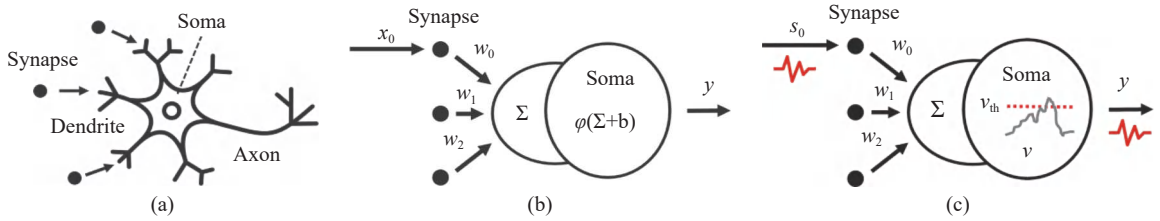

Figure 5 (a) Schematic diagram of a biological neuron; (b) Schematic diagram of an ANN neuron; (c) Schematic diagram of an SNN neuron.

There are various neural dynamics of SNNs currently available, ranging from the simpler integrate-and-fire model (IF) and leaky-integrate-and-fired (LIF) model to the more complex Hodgkin-Huxley (HH) models from biology [11], [12]. However, considering the hardware deployment of SNNs, discrete equations are generally used to describe the spiking neurons. Based on a variety of neuronal dynamics models, the description of a typical neuron mainly includes the three behaviors of accumulation, fire, and reset, which correspond to the following three equations:

$$H(t) = f(V(t-1), X(t)) \tag{1}$$

$$S(t) = \theta(H(t) - V_{\text{th}}) \tag{2}$$

$$V(t) = H(t) \cdot (1 - S(t)) + V_{\text{reset}} \cdot S(t) \tag{3}$$

where t is the time stamp and $V(t)$ and $V(t-1)$ represent the membrane potential at the current and last time, respectively, which are the most important hidden variables in neuronal dynamics. $X(t)$ represents the input at the current moment, which is generally the potential increment caused by pre-synapses. $H(t)$ represents the instantaneous membrane potential before the spike is released at the current moment. V_{th} represents the threshold potential of the neuron, and V_{rest} is the reset voltage. Here, the step function θ is used to indicate whether the current spike transmits the spike signal $S(t)$. The two main differences between neuronal dynamics are the state update equation f and the reset of neurons. Currently, more widely used in neuromorphic computing are LIF neurons, whose discrete form of the neuron state update equation is described as

$$f(V(t-1), X(t)) = V(t-1) + \frac{1}{\tau_m}(-(V(t-1) - V_{\text{reset}}) + X(t)) \tag{4}$$

where τ_m is the time constant describing the decay of the membrane potential, also known as the discount factor.

While LIF neurons are relatively simple, their neuronal dynamics still have reasonable biological plausibility and they have been proven to perform well in most computing task scenarios.

Due to the presence of neuronal dynamics, the behavior of neurons is continuously influenced by a certain time window. Therefore, neuromorphic computing presents better robustness to transient disturbances when deployed for applications. In addition, some studies have combined anatomical studies of biological neurons to enhance the ability of neurons to integrate temporal spikes and thus maintain a more stable performance by introducing mechanisms such as adaptive release thresholds [38], [39]. The neuronal dynamics of SNNs are evolving under the influence of both computational applications and biological inspiration.

3) Deep learning

An essential application of neuromorphic computing is to solve deep learning tasks. Figure 6 illustrates the timeline of major discoveries and advances in intelligent computing from the 1940s to the present [32]. For decades, ANNs have achieved outstanding results in natural language processing, image processing, robot control, and many other fields. Although SNNs can theoretically achieve the exact fitting of nonlinear systems as ANNs by introducing spike coding and neuronal dynamics, the practical performance in such applications needs further discussion.

A deep neural network requires inference and, more importantly, a well-developed training method. ANNs currently adjust network parameters based on gradient information by building loss functions and performing back-propagation of errors. However, because SNNs propagate data through spike signals based on neuronal dynamics, it is challenging to learn similarly from gradient information. Therefore, a common practice is to guarantee training through custom backward gradient propagation rules, also referred to as surrogate gradients [40]. However, surrogate gradients are relatively ambiguous, and thus, the ultimate performance of SNNs becomes challenging to surpass that of ANNs with such training methods. Recent research advances have focused intently on training methods for SNNs, including synthetic gradients or three-factor learning from a biological perspective [41]–[43]. In addition, due to the nature of neuromorphic computing chip storage and computation, some research has focused on hardware-friendly on-chip training methods, such as e-prop, which offer favorable application prospects [44]–[46].

Although there are some key challenges in training SNNs, given the unique advantages of neuromorphic computing and its hardware, deploying SNNs to replace ANNs to achieve more complex tasks is still very promising. Thus, another important advancement for SNNs is to establish their relationship with well-trained ANNs. Such a transformation method focuses on converting an ANN with parameters that have been trained into an effective SNN that can be deployed on a neuromorphic chip [47], [48]. Through these transformation methods, ANN training techniques are also applied, thus avoiding the training problem of deeper

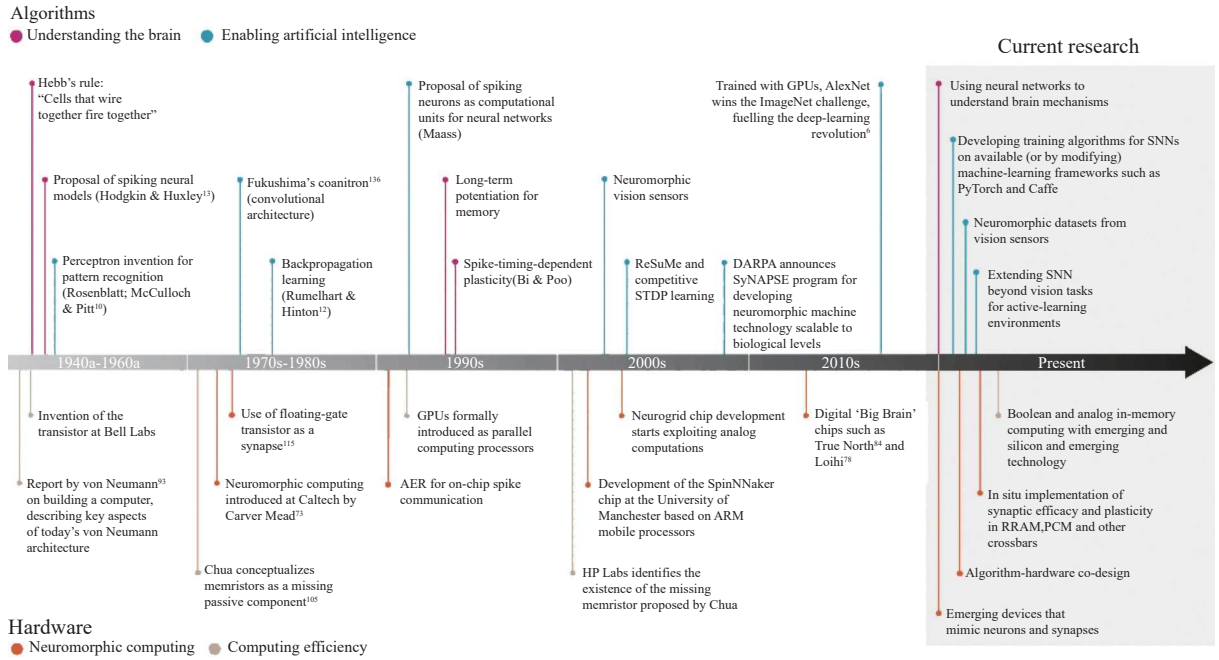

Figure 6 Timeline of major discoveries and advances in intelligent computing from the 1940s to the present [32].

SNNs, and these SNNs obtained by the transformation method also show higher performance than the direct training method in many task scenarios.

However, because one of the starting points of the transformation method is the statistical approximation of the spike, the SNNs obtained from the transformation often use frequency encoding and require a relatively longtime window, which increases the computational latency to some extent [49]. Subsequent studies include combining the conversion method with the direct training method, which effectively shortens the time window and achieves good performance [50]. Because task accuracy is the most important metric, this series of techniques based on the conversion method, linking SNNs with ANNs, is the mainstream and the focus of the research field in the near future.

3. Applications

Due to their respective strengths, ANN and SNN are uniquely positioned in different deep learning application scenarios [51]. Specifically, an ANN is highly abstract in its description of neural systems and shows better accuracy and performance in deep learning. However, due to the memory wall problem of von Neumann architecture, its power and cost are higher. Therefore, this architecture is more suitable for cloud and strong edge-end application scenarios. On the other hand, SNN is a more biological description of the neural system, which has the advantage of relatively lower power and cost with better robustness and thus has great potential in edge computing.

In addition, ANN is more adept at static data pair processing, while SNN processes dynamic information due to neuronal dynamics. For example, ANN is considered relatively more suitable for image and video processing applications, while SNN has unique advantages in areas such as detection and control [52]. Although ANNs are partially inspired by the cerebral cortex in terms of spatial complexity [53], they have been used effectively in many specific applications [54], [55]. Examples of such specific tasks are image recognition and classification [56], natural language processing [57], speech recognition [58], and gaming [59]. On the other hand, SNNs take advantage of event-driven spikes, rich spatiotemporal dynamics, and compact memory and computing elements to offer advantages in terms of energy and computing efficiency. There is growing interest in the application of SNNs in computer vision, as in [48], [60], [61], where SNNs are used for image classification. New vision sensors have been designed that are biologically inspired and show outputs that respond asynchronously to the relative change in the pixel intensity [62], [63], making them compatible with SNNs and paving the way for low-latency, energy efficient, and real-time applications. In robotics, SNNs have been used for different tasks, as in [64]–[67]. Moreover, both ANNs and SNNs could be integrated to produce cross-paradigm models and algorithms in a single platform, resulting in hybrid neural networks (HNNs). [4], [68]. Therefore, ANN and SNN will continue to be developed in the near future and are not substitutes for each other. In addition to the differences in working principles between ANNs and SNNs from cloud to edge, combining their advantages in the same task also requires continuous research and breakthroughs in algorithms and hardware.

III. EMI and SI in Neuromorphic Chips

An advantage of the working mechanism of the human brain neural network lies in the low-frequency spike signals and low power consumption. Correspondingly, the neuromorphic chips that have been manufactured thus far all adopt low-frequency transmission signals. However, with the development of neuromorphic chips, the frequen-

cy of the transmission signals tends to increase. The neuromorphic chip is supposed to operate in complex electromagnetic environments. It is necessary to conduct research on the EMI and SI theory of the neuromorphic chip in advance because it has a non-von Neumann architecture with novel neurological devices whose EMI and SI analysis methods should be different from traditional semiconductor chips.

There are roughly two types of neuromorphic chips: neuromorphic chips based on CMOS technology and neuromorphic chips based on memristors. This section introduces EMI and SI analysis and modeling methods in these two types of neuromorphic chips and mainly focuses on the memristor-based neuromorphic crossbar array because its circuit structure deeply imitates the neural network of the human brain and is totally different from traditional CMOS-based chips. The EMI and SI analysis of the crossbar array is considered to be more unique and challenging.

1. EMI and SI analysis in CMOS-based neuromorphic chips

Similar to traditional chips, CMOS-based neuromorphic chips suffer from many EMI and SI issues, including crosstalk, reflection, impedance mismatch, and interboard resonance. These problems of CMOS-based neuromorphic chips can be mainly attributed to the following aspects: 1) the steep rising edge of the signal leads to an excessively high working frequency, which leads to transmission line effects such as reflection, crosstalk and dispersion; 2) the reduced chip operating voltage makes the signal easily interfered with, resulting in a higher bit error rate; and 3) the higher system integration and narrowed wiring distance cause serious parasitic effects of interconnection and packaging, signal crosstalk intensification, etc. The key to EMI and SI research in CMOS-based neuromorphic chips is to clarify various factors affecting the chip performance and adopt measures to overcome them such that the received signals can maintain corresponding characteristics in the time domain and frequency domain.

2. EMI and SI analysis in memristor-based neuromorphic chips

The memristor-based neuromorphic crossbar array occupies a smaller area with lower power consumption compared to the neuromorphic hardware based on traditional devices. However, the reliability of neuromorphic crossbar arrays is still poor due to unstable device performance, special circuit structure, and high integration. At present, the EMI and SI issues of crossbar arrays that have been widely considered and explored can be roughly divided into two parts [69]–[74]: one is the impact of the variation and nonlinearity of memristors at the device level, and the other is the parasitic effects caused by the interconnections at the circuit level.

The emerging memristor [24] is believed to be an excellent alternative for artificial synapses. It can achieve the weight update process in the neural network with resistive switching behavior. The variability of memristor performance is a major barrier to the manufacture of large-scale crossbar arrays. Like other nanodevices, it suffers from process variations (device-to-device), which may cause nonlinear effects in the resistance adjustment region. Furthermore, it also suffers from temporal variations (cycle-to-cycle) caused by the stochastic intrinsic characteristics of memristor switching dynamics.

The most commonly used memristor array architecture in neuromorphic hardware is the one-transistor and one-resistor (1T1R) array. Transistors in series with memristors facilitate the design of neuromorphic chips. First, the transistor gate voltage sets the current compliance so that it can suppress the overshoot and feedback effects. Second, the transistor size is much larger than the memristor, which provides good isolation between cells and minimizes the crosstalk issue. Third, the transistor also helps eliminate the sneak path in the large-scale memristor array.

The 1T1R array offers advantageous performance and reliability, but the transistor in this design occupies too much area. To achieve a higher integration density, the transistor can be replaced by a two-terminal selector (1S1R) or removed from the array (1R). However, a higher density can cause severe electromagnetic problems; therefore, it is more difficult to design a large-scale neuromorphic circuit based on a 1S1R or 1R [75] structure than a 1T1R structure. The 1R crossbar array structure shown in Figure 7 [76], [77] is further illustrated in this section, while Figure 8 describes several typical SI issues in the crossbar array [78], e.g., crosstalk and sneak path.

When the wire width is on the nanoscale, the effects of interconnect capacitance and inductance can be neglected, and there are two typical SI problems of the crossbar array: IR-drop and sneak-path problems. The IR drop is caused by the interconnect resistance. For a large array, the interconnect resistance is comparable to the memristor resistance so that the write voltage will drop on the wire. In addition, the sneak-path problem that occurs in the read process of the crossbar array is shown in Figure 8. When a memristor cell is selected in the array, the other cells on the same row and column are also half-selected. Therefore, there will be sneak-path currents through those half-selected cells, and the read-out current will be higher than the ideal value.

When the wire width is larger and on the micron scale, the influence of the interconnect resistance decreases, and the parasitic effects in the crossbar array are mainly caused by the interconnect inductance and capacitance. The parasitic effects involve voltage degradation, time delay, overshoot, crosstalk and coupling, which may have a strong influence on the performance of the neuromorphic chip.

3. EMI and SI modeling methods for neuromorphic chips

Accurate circuit modeling of a crossbar array is the foundation of EMI and SI analysis. The crossbar model consists of the memristor model and the interconnect model. The Weber distribution is commonly used for statistical analysis [79],

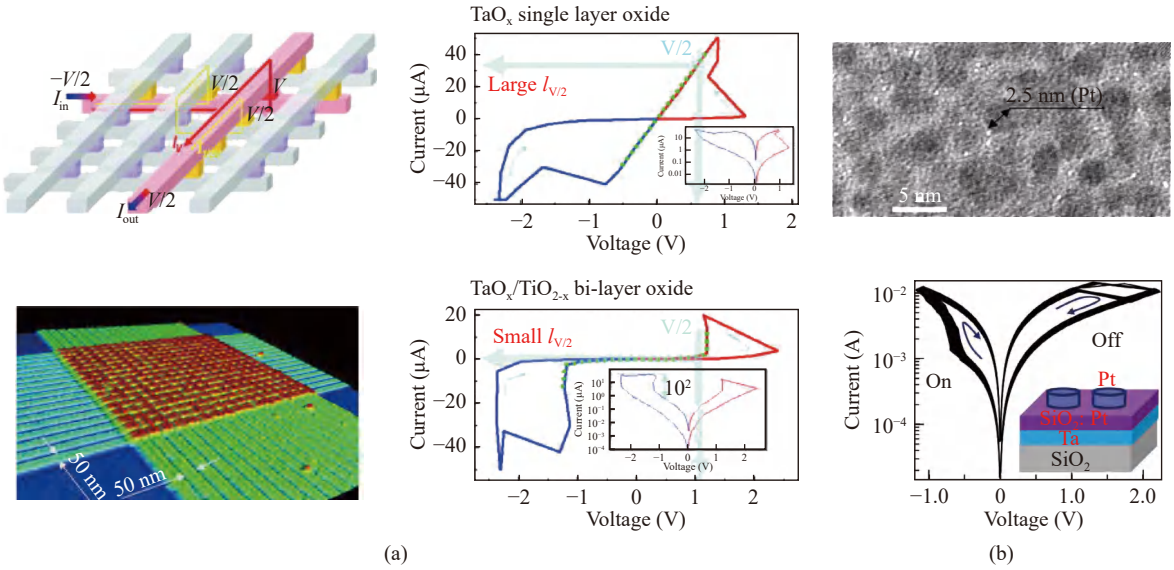

Figure 7 An example of a memristor-based neuromorphic chip. (a) Crossbar array and current voltage loops of a typical memristor nanodevice [76]; (b) TEM image and current-voltage (I-V) switching loops of Pt-dispersed SiO_2 memristor microdevices [77].

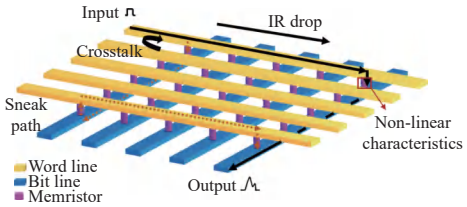

Figure 8 Typical SI issues in memristor-based neuromorphic chips [78].

[80]; however, this type of method does not consider the continuity and high dependence of the random process of memristors. Kinetic Monte-Carlo (KMC) is a powerful method for the numerical modeling of a memristor's intrinsic stochastic switching process [81]–[83]. It can physically describe the forming and rupturing process of the conductive filaments in the memristor. The time series statistical analysis method is also proposed to predict and model the randomness of memristors under continuous periods [84], [85]. However, these methods are very computationally complex and are not suitable for large-scale crossbar array simulations. Compact memristor models for spice simulation have received more attention [86]–[90]. The formation and rupture of the conductive filaments are described by simplified mechanisms.

The crossbar array is usually divided into unit cells for modeling due to its periodic structure. If the size of the crossbar array is on the nanoscale, the interconnect wire can be simply modeled as a resistance. Otherwise, the parasitic inductance and capacitance should also be considered [91]–[97]. Commercial software (e.g., ANSYS Q3D Extractor) can be utilized to extract these parasitic parameters for crossbar array circuits [93]. Meanwhile, calculating parasitic inductance and capacitance by numerical methods can be treated as an alternative method for fast analysis. The partial element equivalent circuit (PEEC) method is one of the most common numerical calculation methods to analyze the parasitic effects of interconnect wires [91], [97]. Figure 9 illustrates the circuit model of the unit cell of a crossbar array, including parasitic inductance, capacitance, and resistance [91]. Since the neural network is realized in the time domain, only the time domain simulation of the crossbar array is discussed. The entire circuit simulation can be conducted in SPICE simulators; however, it is not convenient to simulate a large-scale crossbar array or to implement neural network simulation on the crossbar array. Therefore, it is recommended to conduct simulations by solving circuit matrix functions in programming software such as MATLAB or Python, in which the array size and time loop can be easily modified.

IV. EMI and SI in Heterogeneous Neuromorphic Structures

The term HI was originally used to describe the integration of multifunctional chips at the same location [98]. HI allows stacking of dissimilar components with different feature sizes, functions, materials, or foundries. This gives an advantage over other technologies such as SoC. HI can be achieved through different techniques such as 2D, 2.5D and 3D or other packaging technologies.

The asynchronous nature of the neuromorphic chips benefits real-time and event-based sensory processing, thus featuring low power and latency. In terms of signal processing, the event-driven architecture uses asynchronous design for the inter/intra-chip networking [16], [17]. Nevertheless, clock-domain crossing is inevitable when dealing with synchronous circuits within neuromorphic chips, as in [16], [99], where the neuron computation unit is implemented in a synchronous design style. In such cases, an asynchronous-synchronous interface [100] is required to translate the asynchronous signal to a synchronous signal and vice versa.

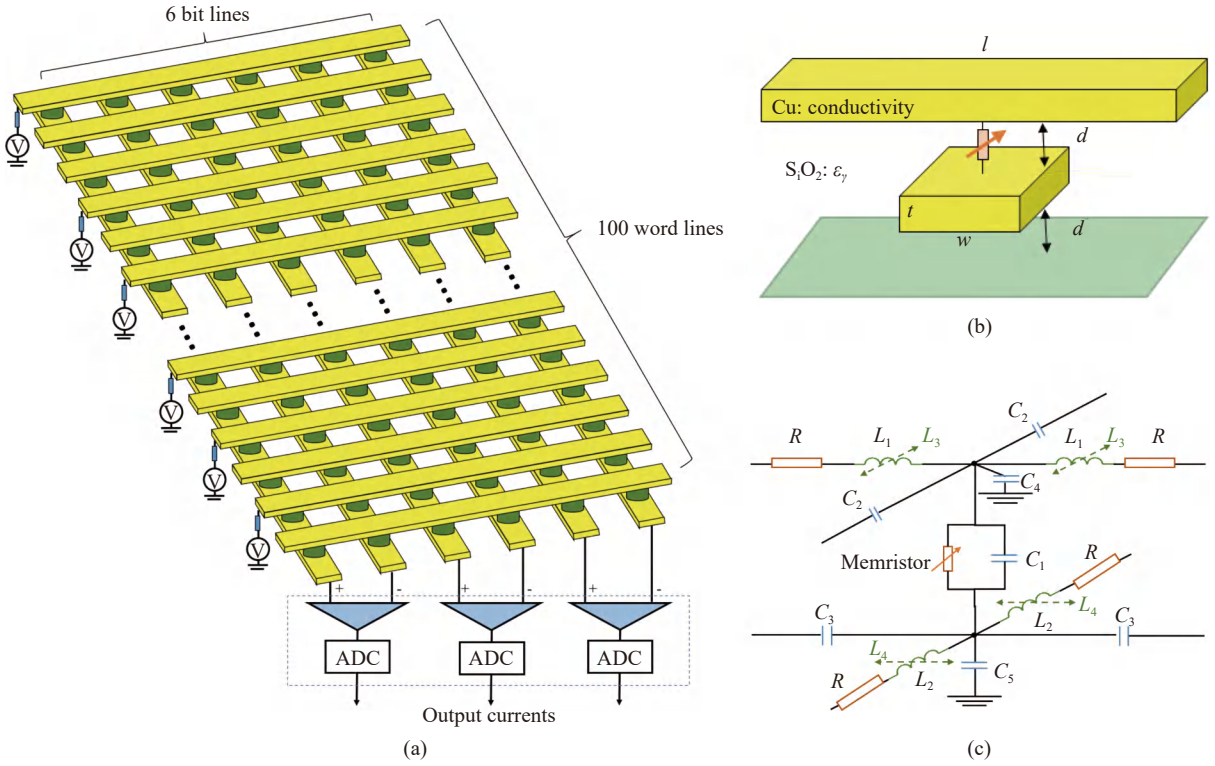

Figure 9 Circuit modeling method for memristor-based neuromorphic chips [91]. (a) Memristor-based neuromorphic chip; (b) and (c) unit cell and equivalent circuit model based on PEEC.

A bidirectional interface between asynchronous and synchronous domains is also required when a neuromorphic chip has been integrated with a traditional chip based on synchronous designs, as shown in Figure 10. HI between neuromorphic circuits and sensors could be achieved using address event representation (AER), as in [101], where a neuromorphic binaural auditory sensor was implemented using FPGA. Similarly, a motion detection (MD) vision sensor using a processing-in-sensor technique yields a high frame rate and low power consumption [102]. In this type of interface, the analog auditory and visual signals are converted into event-based spikes using spike coding schemes and then sent to the AER bus.

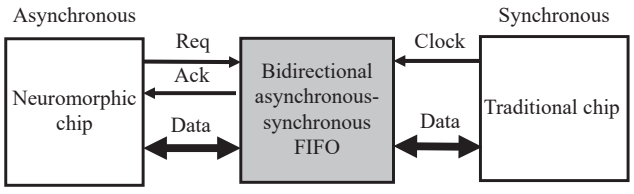

Figure 10 Bidirectional first-in-first-out (FIFO) interface between asynchronous and synchronous domains [100].

HI of neuromorphic circuits and other elements, such as memory arrays and sensors, was achieved through different packaging technologies. For instance, a CMOS image sensor (CIS) and CMOS neurons were fabricated in a single 0.18-μm process chip [103], and the chip was integrated with a memristor array through PCB packaging technology, as shown in Figure 11(a). Although a PCB was successfully used to integrate neuromorphic and sensor circuits, its relatively greater trace length and lower integration density pose significant challenges for modern hardware architectures. In [104], Hartmann *et al.* presented a packet-based AER communication infrastructure to avoid the parallel AER bottleneck. However, field-programmable gate array digital network chip (FPGA-DNC) connections remain susceptible to signal distortion due to the high routing density required by the compact board design. EMI and SI in PCB structures rely on several factors, such as the quality of the PCB trace, wires, connectors, and frequency mismatch. An example of the SI assessment is shown in multi-tile neuromorphic system integrated into a PCB [105], where eye-diagram and bath-tube measurements were conducted to evaluate the SI performance of the links.

Other types of packaging technology, such as SoC, were also used for heterogeneously integrating neuromorphic circuits with different sensors [106], [108]. For the odor classification task, a neuromorphic spiking neural network chip was integrated with an odor sensor. Figure 11(b) shows oflation chip with a die area of 50 mm^2. The chip consists of a neuromorphic circuit with spike timing-dependent plasticity (STDP) learning and an on-chip chemo sensor, with an on-chip sensor interface for signal cancellation, amplification, and filtering. SoC and AER allow the design of large-scale neuromorphic computing systems [11]. However, scaling up the number of neurons and synapses to the billion-device level faces many challenges, such as signal propagation delay, which ultimately degrades the comput-

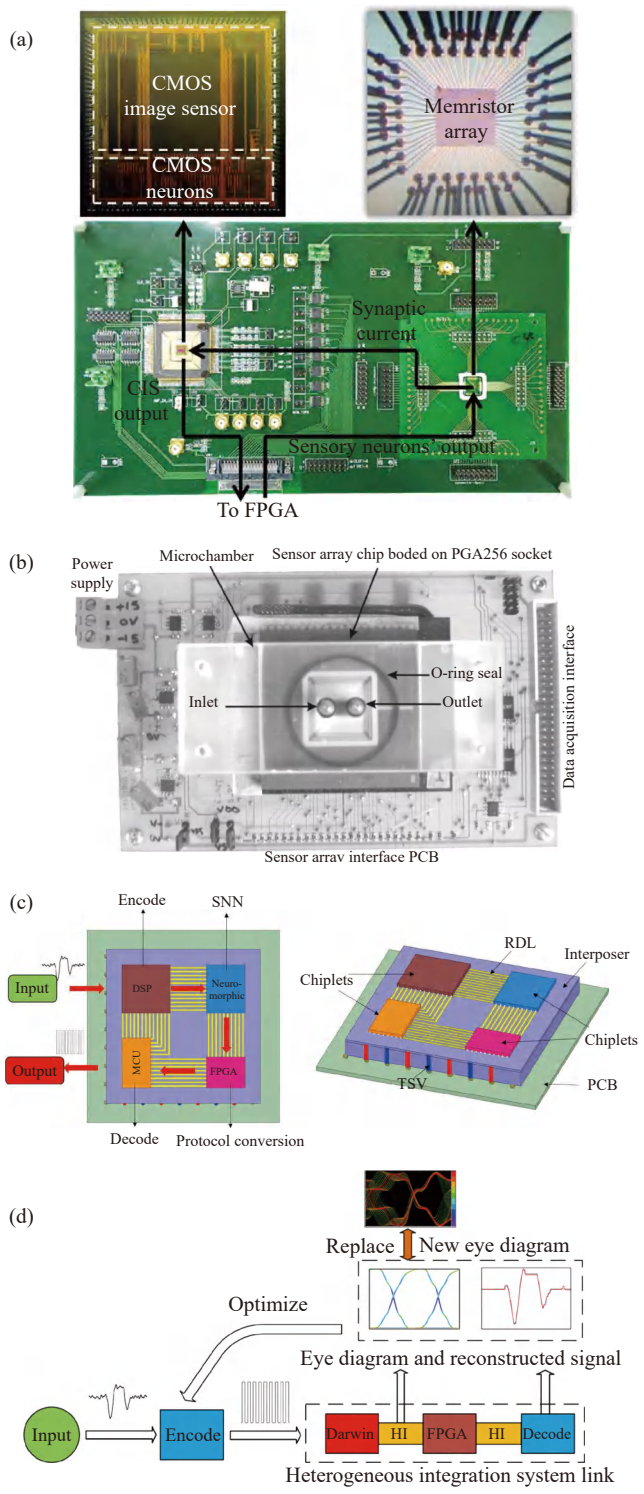

Figure 11 Different types of HI of neuromorphic chips. (a) Neuromorphic system for visual pattern recognition implemented in PCB [103]. (b) The olfaction chip with the chemo-sensor array [106]. Signal link in the heterogeneous system. (c) 2.5-D heterogeneous integrated structure [107]. Initially, the signal is fed to the first subsystem, which mainly comprises a digital signal processing (DSP) chip for chip coding. The coded signal is then fed to the second subsystem, consisting of the Darwin and FPGA chips, which perform SNN operations and data protocol conversion. Finally, the microcontroller unit (MCU) chip outputs the signals. (d) Flow of a novel method for link analysis and result optimization of HI links [107].

ing speed at the system level. Figure 11(c) shows a heterogeneous system of Darwin chip [12] and traditional digital chips in a 2.5D integration structure. The system consists of encoding, neuromorphic chip, and decoding subsystems. Compared to the PCB, 2.5D integration shows less signal loss and jitter [107]. Moreover, novel SI analysis and design methods, such as the use of a two-eye approach, could improve the SI across the link in the 2.5D structure, as shown in Figure 11(d) [107]. Using a two-eyes diagram over a single-eye diagram helps to better understand the SI of the coded signals since the two eyes are both essential and not necessarily equal.

Due to the complexity of neural systems, i.e., high connectivity densities and massive parallelism, 3D HI has been exploited in neuromorphic chips. On the one hand, shorter connections can lower both the energy consumption and latency. On the other hand, 3D stacking offers more connection lines, resulting in an enhanced bandwidth between the layers. 3D HI can take advantage of synaptic crossbars to allow high-density connections, as well as storage of internal information. Belhadj *et al.* [109] integrated a CMOS vision sensor into a neuromorphic accelerator using 130 nm technology. Their sensor was composed of microblock that issues spikes to the neurons using temporal coding [110]. The spikes are passed to the first layer through synaptic weights. The second layer works as a fully connected output classifier layer, as a feature of the parallel connections between the stacked layer in the 3D structure. Copper-to-copper micro-bumps were used for the interlayer connections with a surface area of 5×5 μm^2. Ehsan *et al.* [111] proposed a neuromorphic 3D IC with through silicon vias (TSVs) interconnects. As shown in Figure 12(a), each chip in the 3D structure represents a functional unit. At the bottom of the layout, the CMOS layer represents the neurons, while synapses and axons/dendrites are represented by crossbars and nanowires, respectively. The usage of TSVs (Figure 12(b)) can be extended to other configurations, as explained by Ehsan *et al.* [112]. In particular, redundant and superfluous dummy TSVs were used as membrane capacitors [113], [114]. Such configurations can enhance the performance without increasing the silicon area. The massive parallelism between the adjacent layers in the 3D structure due to the abundant TSVs imposes EMI and SI issues such as crosstalk and electromagnetic coupling. For instance, the presence of adjacent signal TSVs (Figure 12(c)) [115] imposes electromagnetic field coupling as a result of the strong mutual capacitance and inductance between the TSVs. Moreover, the discontinuous structure (Figure 12(d)) and the bump formed at the interconnection of the TSV and redistribution layer (RDL) may lead to signal loss [116]. In fact, this type of discontinuity was found to contribute significant losses to the signal and thus to compromise the EMI and SI.

Recently, Choi *et al.* [117] reported a Lego-like 3D heterogeneous structure of multi-stacked neuromorphic chips. Chip-to-chip communication is achieved by opto-

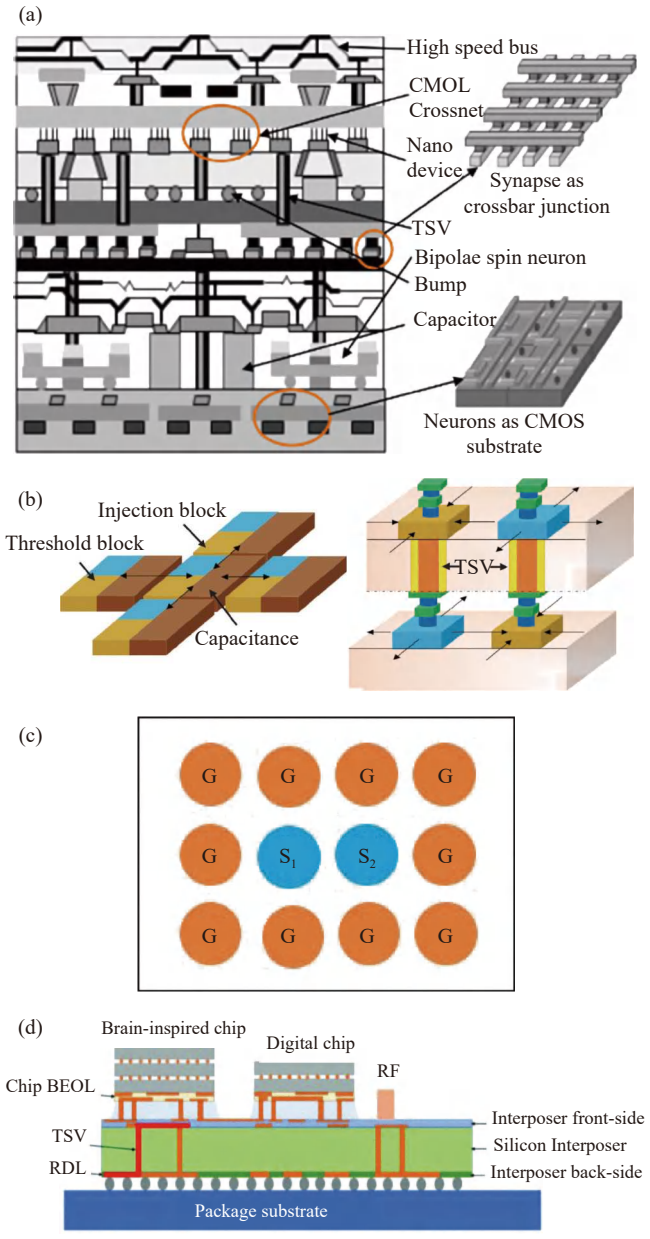

Figure 12 3D HI structure of neuromorphic chips. (a) TSV arrangements between neuron cell layers [111]; (b) TSV and RDL in the 3D HI structure [112]; (c) TSV-based 3D neuromorphic IC [115]; (d) Usage of TSV as a capacitor [116].

electronic device arrays, which not only allow stackability but also allow replaceability of sensors depending on the input. Figure 13(a) shows a schematic of how the eye layer (input layer) sends light to the next layer. Each layer has an optoelectronic device of LED and PD stacks to send and receive the light, respectively (Figure 13(b)). Moreover, a library of sensors, processors, and noise-reducing processors is designed to ensure modular reconfigurable design.

V. Discussion and Future Prospects

Conventional techniques for circuit prediction and optimization, such as Monte Carlo (MC) [118], worst-case [119], parametric macro-modeling [120], [121] and statistics-

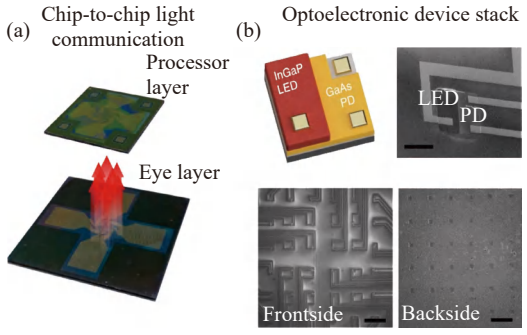

Figure 13 Optoelectronic devices in a 3D HI structure [117]. (a) Optical photograph of the eye layer and processor layer; (b) SEM images of an optoelectronic device stack.

based methods [122], suffer in providing ultimate efficiency with accurate analysis. Emergent prediction and optimization methods such as machine learning (ML) have been used in many engineering fields related to CMOS technology. Using ML methods could help alleviate difficulties related to traditional methods such as electromagnetic solvers [123] and circuit simulators [124]. Although there have been efforts to enhance EMI and SI analysis [125], [126], traditional methods still face many challenges [122]. For IC design and advanced packaging, deep learning has been used to predict EMI and SI performance by using the circuit parameter [127]–[131], resulting in enormous time savings for electronic design automation (EDA) simulations. Figure 14 shows an example of SI prediction for chip-to-chip connections using a neural network [129]. Deep learning methods can be used in forward prediction problems and inverse design problems, i.e., through a mea-

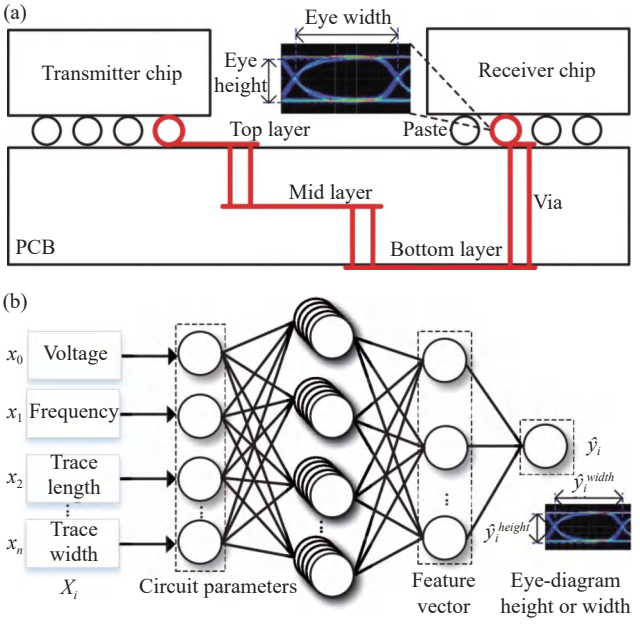

Figure 14 A hybrid neural network (HNN) used to predict the eye diagram metrics [129]. (a) The structure of chip-to-chip connections. (b) The structure of the DNN network. The network takes *n* channel parameters, such as voltage and frequency, as inputs and gives eye-diagram parameters, such as eye height and width, as outputs.

surement such as an eye diagram, designers can identify or classify the circuit defect that causes signal loss or crosstalk [132]. Additionally, EMI and SI optimization could also be achieved, as in [133], where a deep genetic algorithm (GA) was proposed to optimize a high-speed channel.

In memristor-based neuromorphic circuits, various optimization methods have recently been proposed from three aspects: memristor devices, crossbar circuits and neuromorphic computing algorithms. First, the performance of the memristor device should be improved. The adjustment of memristor conductance is preferably stable and linear by adopting special material and process technology [134]. Second, the parameters of the interconnect wire can be modified to decrease the parasitic effects. The crossbar array segmentation method is proposed to flexibly create a combination of various array sizes to design a memristor crossbar array circuit closer to the desired ideal size and reduce the calculation error [135]. It is also necessary to develop multi-parameter optimization methods under the consideration of circuit uncertainties [136]. Third, there is a great demand for the design and enhancement of the brain-like algorithm according to the EMI and SI properties of the neuromorphic chip. A novel sensing training scheme (Vortex) was proposed to actively compensate for the influence of device changes, thus ensuring the reasoning accuracy and enhancing the training robustness of memristor-based neuromorphic circuits [137]. Improved spiking neural network algorithms considering hardware implementation and circuit parasitic effects are also helpful to improve the calculation accuracy and efficiency of the whole circuit [138], [139]. In the future, the co-design of the neural network algorithm and the crossbar array structure would be very helpful. Suitable algorithms may achieve better hardware performance.

Consistent with the post-Moore era, 3D HI is expected to gain more attention to meet the urgent demands for multifunctional neuromorphic chips. Therefore, it is essential to develop approaches to neuromorphic computing that function as close as possible to the sensors, with interlayer connections that allow module versatility and comply with the energy and performance requirements.

In HI of stackable chips using light communication, the accurate alignment between the front and backside of the LED/PD stacks is crucial to ensure EMI and SI performance. In chip-to-chip light communication [117], the alignment of the chips is achieved by using micro-manipulators, together with the deep reactive ion etching technique for patterning.

To cope with the enormous potential of AI in enhancing SI performance and mitigating EMI problems in neuromorphic chips, we propose that both academic and industry institutions will continue driving silicon technologies toward AI-driven EDA tools. The merging of AI techniques into EDA tools is expected to make SI design simpler and less time-consuming. An example of such innovation is Synopsys's new EDA suite: Synopsys.ai, which was recently unveiled as Industry's first full-stack, AI-driven EDA suite for chipmakers [140]. Other EDA companies are expected to explore in the same direction, with more focus on 3D-HI, enhanced chip-to-chip communication, and memristor-based devices.

VI. Conclusion

Neuromorphic chips present a promising solution toward the realization of efficient and robust systems that are motivated by the neurobiological system of the brain. EMI and SI modeling and analysis in neuromorphic chips play a crucial role in determining their performance. This paper reviews EMI and SI issues in both neuromorphic chips and heterogeneous structures. First, neuromorphic chips are briefly reviewed, considering their design, algorithms, and applications. Due to their differences in physical nature, EMI and SI issues in memristor-based chips are discussed separately to better capture these concepts with respect to various memristor-based architectures. HI of the multifunctional chips is inevitable due to the continuous decrease in chip size. Therefore, the effects of EMI and SI in various heterogeneous structures, such as PCB, SoC, 3D, and light connections, are reviewed. Various optimization techniques to enhance the EMI and SI performance are also reviewed, including emergent prediction and optimization methods such as ML methods. Finally, future prospects of EMI and SI optimization methods are discussed.

Acknowledgement

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References

[1] J. McCarthy, M. L. Minsky, N. Rochester, *et al*., "A proposal for the Dartmouth summer research project on artificial intelligence, August 31, 1955," *AI Magazine*, vol. 27, no. 4, pp. 12–14, 2006.

[2] W. Q. Zhang, B. Gao, J. S. Tang, *et al*., "Neuro-inspired computing chips," *Nature Electronics*, vol. 3, no. 7, pp. 371–382, 2020.

[3] A. Krikelis and C. C. Weems, "Associative processing and processors," *Computer*, vol. 27, no. 11, pp. 12–17, 1994.

[4] J. Pei, L. Deng, S. Song, *et al*., "Towards artificial general intelligence with hybrid Tianjic chip architecture," *Nature*, vol. 572, no. 7767, pp. 106–111, 2019.

[5] W. Maass, "Networks of spiking neurons: The third generation of neural network models," *Neural Networks*, vol. 10, no. 9, pp. 1659–1671, 1997.

[6] A. Reuther, P. Michaleas, M. Jones, *et al*., "AI and ML accelerator survey and trends," in *Proceedings of 2022 IEEE High Performance Extreme Computing Conference*, Waltham, MA, USA, pp. 1–10, 2022.

[7] N. K. Huang, L. J. Jiang, H. C. Yu, *et al*., "Fundamental components of the IC packaging electromagnetic interference (EMI) analysis," in *Proceedings of 2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems*, Tempe, AZ, USA, pp. 141–144, 2012.

[8] N. K. H. Huang, L. J. Jiang, H. C. Yu, *et al*., "Electromagnetic

emissions from the IC packaging," in *Proceedings of 2012 IEEE Electrical Design of Advanced Packaging and Systems Symposium*, Taipei, China, pp. 65–68, 2012.

[9] T. Sudo, H. Sasaki, N. Masuda, *et al*., "Electromagnetic interference (EMI) of system-on-package (SOP)," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 304–314, 2004.

[10] A. R. Young, M. E. Dean, J. S. Plank, *et al*., "A review of spiking neuromorphic hardware communication systems," *IEEE Access*, vol. 7, pp. 135606–135620, 2019.

[11] F. Akopyan, J. Sawada, A. Cassidy, *et al*., "TrueNorth: Design and tool flow of a 65 mW 1 million neuron programmable neurosynaptic chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 10, pp. 1537–1557, 2015.

[12] D. Ma, J. C. Shen, Z. H. Gu, *et al*., "Darwin: A neuromorphic hardware co-processor based on spiking neural networks," *Journal of Systems Architecture*, vol. 77, pp. 43–51, 2017.

[13] J. C. Shen, D. Ma, Z. H. Gu, *et al*., "Darwin: A neuromorphic hardware co-processor based on spiking neural networks," *Science China Information Sciences*, vol. 59, no. 2, pp. 1–5, 2016.

[14] M. Bouvier, A. Valentian, T. Mesquida, *et al*., "Spiking neural networks hardware implementations and challenges: A survey," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 15, no. 2, article no. 22, 2019.

[15] S. B. Furber, F. Galluppi, S. Temple, *et al*., "The SpiNNaker project," *Proceedings of the IEEE*, vol. 102, no. 5, pp. 652–665, 2014.

[16] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, *et al*., "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, 2014.

[17] M. Davies, N. Srinivasa, T. H. Lin, *et al*., "Loihi: A neuromorphic manycore processor with on-chip learning," *IEEE Micro*, vol. 38, no. 1, pp. 82–99, 2018.

[18] B. V. Benjamin, P. R. Gao, E. McQuinn, *et al*., "Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations," *Proceedings of the IEEE*, vol. 102, no. 5, pp. 699–716, 2014.

[19] A. Neckar, S. Fok, B. V. Benjamin, T. C. Stewart, *et al*., "Braindrop: A mixed-signal neuromorphic architecture with a dynamical systems-based programming model," *Proceedings of the IEEE*, vol. 107, no. 1, pp. 144–164, 2019.

[20] S. Schmitt, J. Klähn, G. Bellec, *et al*., "Neuromorphic hardware in the loop: Training a deep spiking network on the BrainScaleS wafer-scale system," in *Proceedings of 2017 International Joint Conference on Neural Networks*, Anchorage, AK, USA, pp. 2227–2234, 2017.

[21] J. Schemmel, D. Brüderle, A. Grübl, *et al*., "A wafer-scale neuromorphic hardware system for large-scale neural modeling," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, Paris, France, pp. 1947–1950, 2010.

[22] A. Vanarse, A. Osseiran, A. Rassau, *et al*., "A hardware-deployable neuromorphic solution for encoding and classification of electronic nose data," *Sensors*, vol. 19, no. 22, article no. 4831, 2019.

[23] O. Moreira, A. Yousefzadeh, F. Chersi, *et al*., "NeuronFlow: A hybrid neuromorphic–dataflow processor architecture for AI workloads," in *Proceedings of 2020 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems*, Genova, Italy, pp. 1–5, 2020.

[24] D. B. Strukov, G. S. Snider, D. R. Stewart, *et al*., "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[25] W. E. Wan, R. Kubendran, C. Schaefer, *et al*., "A compute-in-memory chip based on resistive random-access memory," *Nature*, vol. 608, no. 7923, pp. 504–512, 2022.

[26] T. F. Wu, H. T. Li, P. C. Huang, *et al*., "Hyperdimensional computing exploiting carbon nanotube FETs, resistive RAM, and their monolithic 3D integration," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3183–3196, 2018.

[27] K. Prabhu, A. Gural, Z. F. Khan, *et al*., "CHIMERA: A 0.92-TOPS, 2.2-TOPS/W edge AI accelerator with 2-MByte on-chip foundry resistive RAM for efficient training and inference," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 4, pp. 1013–1026, 2022.

[28] Y. Zha, E. Nowak, and J. Li, "Liquid silicon: A nonvolatile fully programmable processing-in-memory processor with monolithically integrated ReRAM," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 908–919, 2020.

[29] M. Y. Chang, A. S. Lele, S. D. Spetalnick, *et al*., "A 73.53TOPS/W 14.74TOPS heterogeneous RRAM in-memory and SRAM near-memory SoC for hybrid frame and event-based target tracking," in *Proceedings of 2023 IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, pp. 426–428, 2023.

[30] S. Pi, C. Li, H. Jiang, *et al*., "Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension," *Nature Nanotechnology*, vol. 14, no. 1, pp. 35–39, 2019.

[31] P. Lin, C. Li, Z. R. Wang, *et al*., "Three-dimensional memristor circuits as complex neural networks," *Nature Electronics*, vol. 3, no. 4, pp. 225–232, 2020.

[32] K. Roy, A. Jaiswal, and P. Panda, "Towards spike-based machine intelligence with neuromorphic computing," *Nature*, vol. 575, no. 7784, pp. 607–617, 2019.

[33] D. Auge, J. Hille, E. Mueller, *et al*., "A survey of encoding techniques for signal processing in spiking neural networks," *Neural Processing Letters*, vol. 53, no. 6, pp. 4693–4710, 2021.

[34] R. Massa, A. Marchisio, M. Martina, *et al*., "An efficient spiking neural network for recognizing gestures with a DVS camera on the Loihi neuromorphic processor," in *Proceedings of 2020 International Joint Conference on Neural Networks*, Glasgow, UK, pp. 1–9, 2020.

[35] G. Cohen, S. Afshar, B. Morreale, *et al*., "Event-based sensing for space situational awareness," *The Journal of the Astronautical Sciences*, vol. 66, no. 2, pp. 125–141, 2019.

[36] T. B. Brown, B. Mann, N. Ryder, *et al*., "Language models are few-shot learners," in *Proceedings of the 34th International Conference on Neural Information Processing Systems*, Vancouver, Canada, article no.159, 2020.

[37] A. Tavanaei, M. Ghodrati, S. R. Kheradpisheh, *et al*., "Deep learning in spiking neural networks," *Neural Networks*, vol. 111, pp. 47–63, 2019.

[38] C. T. Yu, Z. M. Gu, D. Li, *et al*., "STSC-SNN: Spatio-temporal synaptic connection with temporal convolution and attention for spiking neural networks," *Frontiers in Neuroscience*, vol. 16, article no. 1079357, 2022.

[39] R. J. Zhu, Q. H. Zhao, T. J. Zhang, *et al*., "TCJA-SNN: Temporal-channel joint attention for spiking neural networks," *arXiv preprint*, arXiv: 2206.10177, 2022.

[40] Y. J. Wu, L. Deng, G. Q. Li, *et al*., "Spatio-temporal backpropagation for training high-performance spiking neural networks," *Frontiers in Neuroscience*, vol. 12, article no. 331, 2018.

[41] A. Kohan, E. A. Rietman, and H. T. Siegelmann, "Forward signal propagation learning," *arXiv preprint*, arXiv: 2204.01723, 2022.

[42] A. Nøkland and L. H. Eidnes, "Training neural networks with local error signals," in *Proceedings of the 36th International Conference on Machine Learning*, Long Beach, CA, USA, pp. 4839–4850, 2019.

[43] J. Kaiser, H. Mostafa, and E. Neftci, "Synaptic plasticity dynamics for deep continuous local learning (DECOLLE)," *Frontiers in Neuroscience*, vol. 14, article no. 424, 2020.

[44] F. M. Quintana, F. Perez-Peña, P. L. Galindo, *et al*., "ETLP: Event-based three-factor local plasticity for online learning with neuromorphic hardware," *arXiv preprint*, arXiv: 2301.08281, 2023.

[45] G. Bellec, F. Scherr, A. Subramoney, *et al*., "A solution to the

learning dilemma for recurrent networks of spiking neurons," *Nature Communications*, vol. 11, no. 1, article no. 3625, 2020.

[46] A. Perrett, S. Summerton, A. Gait, *et al*., "Online learning in SNNs with e-prop and neuromorphic hardware," in *Proceedings of the 2022 Annual Neuro-Inspired Computational Elements Conference*, Virtual Event, USA, pp. 32–39, 2022.

[47] P. U. Diehl, G. Zarrella, A. Cassidy, *et al*., "Conversion of artificial recurrent neural networks to spiking neural networks for low-power neuromorphic hardware," in *Proceedings of 2016 IEEE International Conference on Rebooting Computing*, San Diego, CA, USA, pp. 1–8, 2016.

[48] B. Rueckauer, I. A. Lungu, Y. H. Hu, *et al*., "Conversion of continuous-valued deep networks to efficient event-driven networks for image classification," *Frontiers in Neuroscience*, vol. 11, article no. 682, 2017.

[49] Y. J. Wu, L. Deng, G. Q. Li, *et al*., "Direct training for spiking neural networks: Faster, larger, better," in *Proceedings of the 33rd AAAI Conference on Artificial Intelligence*, Honolulu, HI, USA, pp. 1311–1318, 2019.

[50] N. Rathi, G. Srinivasan, P. Panda, *et al*., "Enabling deep spiking neural networks with hybrid conversion and spike timing dependent backpropagation," in *Proceedings of the 8th International Conference on Learning Representations*, Addis Ababa, Ethiopia, 2020.

[51] D. A. Nguyen, X. T. Tran, and F. Iacopi, "A review of algorithms and hardware implementations for spiking neural networks," *Journal of Low Power Electronics and Applications*, vol. 11, no. 2, article no. 23, 2021.

[52] K. Yamazaki, V. K. Vo-Ho, D. Bulsara, *et al*., "Spiking neural networks and their applications: A review," *Brain Sciences*, vol. 12, no. 7, article no. 863, 2022.

[53] G. Qiu, "Modelling the visual cortex using artificial neural networks for visual image reconstruction," in *Proceedings of 1995 Fourth International Conference on Artificial Neural Networks*, Cambridge, UK, 1995.

[54] Y. LeCun, Y. Bengio, and G. Hinton, "Deep learning," *Nature*, vol. 521, no. 7553, pp. 436–444, 2015.

[55] S. J. Russell and P. Norvig, *Artificial Intelligence: A Modern Approach*, 3rd ed. , Pearson Education Limited, Essex, England, 2016.

[56] K. M. He, X. Y. Zhang, S. Q. Ren, *et al*., "Deep residual learning for image recognition," in *Proceedings of 2016 IEEE Conference on Computer Vision and Pattern Recognition*, Las Vegas, NV, USA, pp. 770–778, 2016.

[57] T. Young, D. Hazarika, S. Poria, *et al*., "Recent trends in deep learning based natural language processing [Review Article]," *IEEE Computational Intelligence Magazine*, vol. 13, no. 3, pp. 55–75, 2018.

[58] G. Hinton, L. Deng, D. Yu, *et al*., "Deep neural networks for acoustic modeling in speech recognition: The shared views of four research groups," *IEEE Signal Processing Magazine*, vol. 29, no. 6, pp. 82–97, 2012.

[59] D. Silver, A. Huang, C. J. Maddison, *et al*., "Mastering the game of go with deep neural networks and tree search," *Nature*, vol. 529, no. 7587, pp. 484–489, 2016.

[60] E. Hunsberger and C. Eliasmith, "Training spiking deep networks for neuromorphic hardware," *arXiv preprint*, arXiv: 1611.05141, 2016.

[61] A. Sengupta, Y. Ye, R. Wang, *et al*., "Going deeper in spiking neural networks: VGG and residual architectures," *Frontiers in Neuroscience*, vol. 13, article no. 95, 2019.

[62] P. Lichtsteiner, C. Posch, and T. Delbruck, "A 128 × 128 120 dB 15 μs latency asynchronous temporal contrast vision sensor," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 566–576, 2008.

[63] S. Mafrica, S. Godiot, M. Menouni, *et al*., "A bio-inspired analog silicon retina with michaelis-menten auto-adaptive pixels sensitive to small and large changes in light," *Optics Express*, vol. 23, no. 5, pp. 5614–5635, 2015.

[64] J. Dupeyroux, J. J. Hagenaars, F. Paredes-Vallés, *et al*., "Neuromorphic control for optic-flow-based landing of MAVs using the Loihi processor," in *Proceedings of 2021 IEEE International Conference on Robotics and Automation*, Xi'an, China, pp. 96–102, 2021.

[65] E. Angelidis, E. Buchholz, J. Arreguit, *et al*., "A spiking central pattern generator for the control of a simulated lamprey robot running on SpiNNaker and Loihi neuromorphic boards," *Neuromorphic Computing and Engineering*, vol. 1, no. 1, article no. 014005, 2021.

[66] E. Donati, F. Corradi, C. Stefanini, *et al*., "A spiking implementation of the lamprey's central pattern generator in neuromorphic VLSI," in *Proceedings of 2014 IEEE Biomedical Circuits and Systems Conference*, Lausanne, Switzerland, pp. 512–515, 2014.

[67] D. Gutierrez-Galan, J. P. Dominguez-Morales, F. Perez-Peña, *et al*., "Neuropod: A real-time neuromorphic spiking CPG applied to robotics," *Neurocomputing*, vol. 381, pp. 10–19, 2019.

[68] A. Kugele, T. Pfeil, M. Pfeiffer, *et al*., "Hybrid SNN-ANN: Energy-efficient classification and object detection for event-based vision," in *Proceedings of the 43rd DAGM German Conference on Pattern Recognition*, Bonn, Germany, pp. 297–312, 2021.

[69] D. Vaidya, S. Kothari, T. Abbey, *et al*., "Compact modeling of the switching dynamics and temperature dependencies in TiO_x-Based memristors—Part I: Behavioral model," *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 4877–4884, 2021.

[70] O. Krestinskaya, K. N. Salama, and A. P. James, "Learning in memristive neural network architectures using analog backpropagation circuits," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 66, no. 2, pp. 719–732, 2019.

[71] Y. Zhang, X. P. Wang, and E. G. Friedman, "Memristor-based circuit design for multilayer neural networks," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 65, no. 2, pp. 677–686, 2018.

[72] P. Yao, H. Q. Wu, B. Gao, *et al*., "Face classification using electronic synapses," *Nature Communications*, vol. 8, no. 1, article no. 15199, 2017.

[73] P. Yao, H. Q. Wu, B. Gao, *et al*., "Fully hardware-implemented memristor convolutional neural network," *Nature*, vol. 577, no. 7792, pp. 641–646, 2020.

[74] S. Jain, A. Sengupta, K. Roy, *et al*., "RxNN: A framework for evaluating deep neural networks on resistive crossbars," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 2, pp. 326–338, 2021.

[75] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, *et al*., "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, no. 7550, pp. 61–64, 2015.

[76] J. J. Yang, M. X. Zhang, M. D. Pickett, *et al*., "Engineering nonlinearity into memristors for passive crossbar applications," *Applied Physics Letters*, vol. 100, no. 11, article no. 113501, 2012.

[77] B. J. Choi, A. C. Torrezan, K. J. Norris, *et al*., "Electrical performance and scalability of Pt dispersed SiO_2 nanometallic resistance switch," *Nano Letters*, vol. 13, no. 7, pp. 3213–3217, 2013.

[78] H. Ma, T. Tao, Q. Chen, *et al*., "Recent progress on signal integrity modeling of neuromorphic chips by the PEEC method," in *Proceedings of 2023 IEEE 32nd Conference on Electrical Performance of Electronic Packaging and System*, accepted, 2023.

[79] S. B. Long, C. Cagli, D. Ielmini, *et al*., "Analysis and modeling of resistive switching statistics," *Journal of Applied Physics*, vol. 111, no. 7, article no. 074508, 2012.

[80] W. C. Luo, J. C. Liu, H. T. Feng, *et al*., "RRAM SET speed-disturb dilemma and rapid statistical prediction methodology," in *Proceedings of 2012 International Electron Devices Meeting*, San Francisco, CA, USA, pp. 9–5, 2012.

[81] S. M. Yu, X. M. Guan, and H. S. P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," in *Proceedings of 2011 International Electron Devices Meeting*, Washington, DC, USA, pp. 17–3, 2011.

[82] S. M. Yu, X. M. Guan, and H. S. P. Wong, "Understanding metal oxide RRAM current overshoot and reliability using kinetic Monte Carlo simulation," in *Proceedings of 2012 International Electron Devices Meeting*, San Francisco, CA, USA, pp. 26.1.1–26.1.4, 2012.

[83] A. Padovani, L. Larcher, O. Pirrotta, *et al*., "Microscopic modeling of HfO_x RRAM operations: From forming to switching," *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1998–2006, 2015.

[84] F. J. Alonso, D. Maldonado, A. M. Aguilera, *et al*., "Memristor variability and stochastic physical properties modeling from a multivariate time series approach," *Chaos, Solitons & Fractals*, vol. 143, article no. 110461, 2021.

[85] J. Roldán, F. J. Alonso, A. M. Aguilera, *et al*., "Time series statistical analysis: A powerful tool to evaluate the variability of resistive switching memories," *Journal of Applied Physics*, vol. 125, no. 17, article no. 174504, 2019.

[86] R. H. Zhu, S. Chang, H. Wang, *et al*., "A versatile and accurate compact model of memristor with equivalent resistor topology," *IEEE Electron Device Letters*, vol. 38, no. 10, pp. 1367–1370, 2017.

[87] H. Nili, A. F. Vincent, M. Prezesio, *et al*., "Comprehensive compact phenomenological modeling of integrated metal-oxide memristors," *IEEE Transactions on Nanotechnology*, vol. 19, pp. 344–349, 2020.

[88] A. S. Demirkol, A. Ascoli, I. Messaris, *et al*., "A compact and continuous reformulation of the Strachan TaO_x memristor model with improved numerical stability," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 69, no. 3, pp. 1266–1277, 2022.

[89] F. Garcia-Redondo, R. P. Gowers, A. Crespo-Yepes, *et al*., "SPICE compact modeling of bipolar/unipolar memristor switching governed by electrical thresholds," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 63, no. 8, pp. 1255–1264, 2016.

[90] Y. Zhao, C. Fang, X. M. Zhang, *et al*., "A compact model for drift and diffusion memristor applied in neuron circuits design," *IEEE Transactions on Electron Devices*, vol. 65, no. 10, pp. 4290–4296, 2018.

[91] T. M. Tao, H. Z. Ma, Q. K. Chen, *et al*., "Circuit modeling for RRAM-based neuromorphic chip crossbar array with and without write-verify scheme," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 68, no. 5, pp. 1906–1916, 2021.

[92] K. Agarwal, D. Sylvester, and D. Blaauw, "Modeling and analysis of crosstalk noise in coupled RLC interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 892–901, 2006.

[93] M. E. Fouda, A. M. Eltawil, and F. Kurdahi, "Modeling and analysis of passive switching crossbar arrays," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 65, no. 1, pp. 270–282, 2018.

[94] S. A. Thomas, S. K. Vohra, R. Kumar, *et al*., "Analysis of parasitic effects in a crossbar in CMOS based neuromorphic system for pattern recognition using memristive synapses," *IEEE Transactions on Nanotechnology*, vol. 21, pp. 380–389, 2022.

[95] Y. Jeong, M. A. Zidan, and W. D. Lu, "Parasitic effect analysis in memristor-array-based neuromorphic systems," *IEEE Transactions on Nanotechnology*, vol. 17, no. 1, pp. 184–193, 2018.

[96] N. Lupo, E. Pérez, C. Wenger, *et al*., "Analysis of parasitic effects in filamentary-switching memristive memories using an approximated Verilog-a memristor model," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 66, no. 5, pp. 1935–1947, 2019.

[97] Y. Li, L. D. Fang, T. M. Tao, *et al*., "Modeling and signal integrity analysis of RRAM-based neuromorphic chip crossbar array using partial equivalent element circuit (PEEC) method," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 69, no. 9, pp. 3490–3500, 2022.

[98] B. Bayraktaroglu, "Heterogeneous integration technology," AFRL/RYDD, Wright Patterson AFB, *Report*, no. AFRL-RY-WP-TR-2017-0168, 2017.

[99] S. G. Cho, E. Beigné, and Z. Y. Zhang, "A 2048-neuron spiking neural network accelerator with neuro-inspired pruning and asynchronous network on chip in 40nm CMOS," in *Proceedings of 2019 IEEE Custom Integrated Circuits Conference*, Austin, TX, USA, pp. 1–4, 2019.

[100] M. Ahmed, E. Li, and Q. Chen, "Bidirectional asynchronous –synchronous FIFO adapter," *Patent*, vol. 202110887132.0, article no. ZL, 2022.

[101] A. Jiménez-Fernández, E. Cerezuela-Escudero, L. Miró-Amarante, *et al*., "A binaural neuromorphic auditory sensor for FPGA: A spike signal processing approach," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 28, no. 4, pp. 804–818, 2017.

[102] T. H. Hsu, Y. K. Chen, M. Y. Chiu, *et al*., "A 0.8 V multimode vision sensor for motion and saliency detection with Ping-Pong PWM pixel," *IEEE Journal of Solid-State Circuits, vol. 56*, no. 8, pp. 2516–2524, 2021.

[103] M. Chu, B. Kim, S. Park, *et al*., "Neuromorphic hardware system for visual pattern recognition with memristor array and CMOS neuron," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2410–2419, 2015.

[104] S. Hartmann, S. Schiefer, S. Scholze, *et al*., "Highly integrated packet-based AER communication infrastructure with 3Gevent/s throughput," in *Proceedings of 2010 17th IEEE International Conference on Electronics, Circuits and Systems*, Athens, Greece, pp. 950–953, 2010.

[105] M. Jabłoński, T. Serrano-Gotarredona, and B. Linares-Barranco, "High-speed serial interfaces for event-driven neuromorphic systems," in *Proceedings of 2015 International Conference on Event-based Control, Communication, and Signal Processing*, Krakow, Poland, pp. 1–4, 2015.

[106] T. J. Koickal, A. Hamilton, S. L. Tan, *et al*., "Analog VLSI circuit implementation of an adaptive neuromorphic olfaction chip," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 54, no. 1, pp. 60–73, 2007.

[107] Q. Chen, D. Li, H. Ma, *et al*., "Hybrid signal integrity modeling and analysis of heterogeneous integrated system with neuromorphic Darwin chip," *IEEE Transactions on Signal and Power Integrity*, under review, 2023.

[108] H. Y. Hsieh and K. T. Tang, "VLSI implementation of a bio-inspired olfactory spiking neural network," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 23, no. 7, pp. 1065–1073, 2012.

[109] B. Belhadj, A. Valentian, P. Vivet, *et al*., "The improbable but highly appropriate marriage of 3D stacking and neuromorphic accelerators," in *Proceedings of the 2014 International Conference on Compilers, Architecture and Synthesis for Embedded Systems*, Uttar Pradesh, India, pp. 1–9, 2014.

[110] P. Lichtsteiner, C. Posch, and T. Delbruck, "A 128 X 128 120dB 30mw asynchronous vision sensor that responds to relative intensity change," in *Proceedings of 2006 IEEE International Solid State Circuits Conference-Digest of Technical Papers*, San Francisco, CA, USA, pp. 2060–2069, 2006.

[111] A. Ehsan, Z. Zhou, and Y. Yi, "Neuromorphic 3D integrated circuit: A hybrid, reliable and energy efficient approach for next generation computing," in *Proceedings of the on Great Lakes Symposium on VLSI 2017*, Banff Alberta, Canada, pp. 221–226, 2017.

[112] M. A. Ehsan, H. Y. An, Z. Zhou, *et al*., "A novel approach for us-

ing TSVs as membrane capacitance in neuromorphic 3-D IC," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 8, pp. 1640–1653, 2018.

[113] U. R. Tida, C. Zhuo, and Y. Y. Shi, "Novel through-silicon-via inductor-based on-chip DC-DC converter designs in 3D ICs," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 11, no. 2, article no. 16, 2014.

[114] A. Joubert, M. Duranton, B. Belhadj, *et al*., "Capacitance of TSVs in 3-D stacked chips a problem? Not for neuromorphic systems!," in *Proceedings of the DAC Design Automation Conference 2012*, San Francisco, CA, USA, pp. 1264–1265, 2012.

[115] M. A. Ehsan, Z. Zhou, and Y. Yi, "Three dimensional integration technology applied to neuromorphic hardware implementation," in *Proceedings of 2015 IEEE International Symposium on Nanoelectronic and Information Systems*, Indore, India, pp. 203–206, 2015.

[116] H. Y. Yu, Z. Sun, X. Y. Lei, *et al*., "Analysis of neural spike signal transmission characteristics in 3-D heterogeneous integration," in *Proceedings of the 2022 Asia-Pacific International Symposium on Electromagnetic Compatibility*, Beijing, China, pp. 91–93, 2022.

[117] C. Choi, H. Kim, J. H. Kang, *et al*., "Reconfigurable heterogeneous integration using stackable chips with embedded artificial intelligence," *Nature Electronics*, vol. 5, no. 6, pp. 386–393, 2022.

[118] R. Spence and R. S. Soin, *Tolerance Design of Electronic Circuits,* World Scientific, 1997.

[119] R. Trinchero, P. Manfredi, T. Y. Ding, *et al*., "Combined parametric and worst case circuit analysis via Taylor models," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 63, no. 7, pp. 1067–1078, 2016.

[120] E. R. Samuel, L. Knockaert, F. Ferranti, *et al*., "Guaranteed passive parameterized macromodeling by using Sylvester state-space realizations," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1444–1454, 2013.

[121] S. Grivet-Talocia and R. Trinchero, "Behavioral, parameterized, and broadband modeling of wired interconnects with internal discontinuities," *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 1, pp. 77–85, 2018.

[122] G. B. Shan, G. L. Li, Y. X. Wang, *et al*., "Application and prospect of artificial intelligence methods in signal integrity prediction and optimization of microsystems," *Micromachines*, vol. 14, no. 2, article no. 344, 2023.

[123] Y. X. Zhang, S. J. Yu, D. Q. Su, *et al*., "Finite element modeling on electromigration of TSV interconnect in 3D package," in *Proceedings of 2018 IEEE 20th Electronics Packaging Technology Conference*, Singapore, Singapore, pp. 695–698, 2018.

[124] A. E. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 22, no. 3, pp. 216–221, 1974.

[125] S. Choi, H. Kim, K. Kim, *et al*., "Signal integrity analysis of silicon/glass/organic interposers for 2.5D/3D interconnects," *in Proceedings of 2017 IEEE 67th Electronic Components and Technology Conference*, vol. Orlando,FL,USA, pp. 2139–2144, 2017.

[126] D. Drogoudis, J. Van Hese, B. Boesman, *et al*., "Combined circuit/full-wave simulations for electromagnetic immunity studies based on an extended S-parameter formulation," in *Proceedings of 2014 IEEE 18th Workshop on Signal and Power Integrity*, Ghent, Belgium, pp. 1–4, 2014.

[127] T. J. Lu, J. Sun, K. Wu, *et al*., "High-speed channel modeling with machine learning methods for signal integrity analysis," *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 6, pp. 1957–1964, 2018.

[128] C. H. Goay, A. Abd Aziz, N. S. Ahmad, *et al*., "Eye diagram contour modeling using multilayer perceptron neural networks with adaptive sampling and feature selection," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 12, pp. 2427–2441, 2019.

[129] S. Y. Chen, J. N. Chen, T. R. Zhang, *et al*., "Semi-supervised learning based on hybrid neural network for the signal integrity analysis," *IEEE Transactions on Circuits and Systems II:Express Briefs*, vol. 67, no. 10, pp. 1934–1938, 2020.

[130] H. Jin, H. Z. Ma, M. D. Butala, *et al*., "EMI radiation prediction and structure optimization of packages by deep learning," *IEEE Access*, vol. 7, pp. 93772–93780, 2019.

[131] H. Z. Ma, E. P. Li, A. C. Cangellaris, *et al*., "Support vector regression-based active subspace (SVR-AS) modeling of high-speed links for fast and accurate sensitivity analysis," *IEEE Access*, vol. 8, pp. 74339–74348, 2020.

[132] W. Y. Miao, C. S. Tan, and M. D. Rotaru, "Eye diagram analysis with deep neural networks for signal integrity applications," in *Proceedings of 2022 IEEE 24th Electronics Packaging Technology Conference*, Singapore, Singapore, pp. 212–217, 2022.

[133] H. H. Zhang, Z. S. Xue, X. Y. Liu, *et al*., "Optimization of high-speed channel for signal integrity with deep genetic algorithm," *IEEE Transactions on Electromagnetic Compatibility*, vol. 64, no. 4, pp. 1270–1274, 2022.

[134] J. L. Meng, Z. H. Li, Y. Q. Fang, *et al*., "Li-ion doped artificial synaptic memristor for highly linear neuromorphic computing," *IEEE Electron Device Letters*, vol. 43, no. 12, pp. 2069–2072, 2022.

[135] D. J. Mountain, M. R. McLean, and C. D. Krieger, "Memristor crossbar tiles in a flexible, general purpose neural processor," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 8, no. 1, pp. 137–145, 2018.

[136] H. Z. Ma, D. Li, T. M. Tao, *et al*., "Uncertainty quantification of signal integrity analysis for neuromorphic chips," *IEEE Transactions on Signal and Power Integrity*, vol. 1, pp. 160–169, 2022.

[137] B. Y. Liu, H. Li, Y. R. Chen, *et al*., "Vortex: Variation-aware training for memristor X-bar," in *Proceedings of the 52nd ACM/EDAC/IEEE Design Automation Conference*, San Francisco, CA, pp. 1–6, 2015.

[138] T. M. Tao, H. Z. Ma, D. Li, *et al*., "Modeling and analysis of spike signal sequence for memristor crossbar array in neuromorphic chips," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 70, no. 6, pp. 2271–2282, 2023.

[139] T. M. Tao, D. Li, H. Z. Ma, *et al*., "A new pre-conditioned STDP rule and its hardware implementation in neuromorphic crossbar array," *Neurocomputing*, vol. 557, article no. 126682, 2023.

[140] Synopsys, "Synopsys. AI unveiled as industry's first full-stack, AI-driven EDA suite for chipmakers," Available at: *https://news.synopsys.com/2023-03-29-Synopsys-ai-Unveiled-as-Industrys-First-Full-Stack,-AI-Driven-EDA-Suite-for-Chipmakers*, 2023-03-29.

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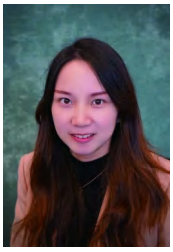

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